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Published in:
Applied Physics Letters

DOI:
[10.1063/1.104866](https://doi.org/10.1063/1.104866)

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Document Version
Publisher's PDF, also known as Version of record

Publication date:
1991

[Link to publication in University of Groningen/UMCG research database](#)

Citation for published version (APA):

van Huffelen, W. M., de Boer, M. J., & Klapwijk, T. M. (1991). Ultrathin silicon membranes to study supercurrent transport in crystalline semiconductors. *Applied Physics Letters*, 58(21), 2438-2440.
<https://doi.org/10.1063/1.104866>

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Citation: *Appl. Phys. Lett.* **58**, 2438 (1991); doi: 10.1063/1.104866

View online: <https://doi.org/10.1063/1.104866>

View Table of Contents: <http://aip.scitation.org/toc/apl/58/21>

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The image shows a Lake Shore Measure Ready 155 Precision I/V Source. The device is a silver, rack-mountable unit with a large color display on the left and control knobs on the right. The display shows 'AC Peak Amplitude 10.0000 mV', 'Frequency 100.000 kHz', and 'DC Offset 0.0000 mV'. The Lake Shore logo is visible on the top left of the device.

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Ultrathin silicon membranes to study supercurrent transport in crystalline semiconductors

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(Received 12 November 1990; accepted for publication 26 February 1991)

We have developed a two-step anisotropic etching process to fabricate thin silicon membranes, used to study supercurrent transport in semiconductor coupled weak links. The process uses a shallow BF_2^+ implantation, and permits easy control of membrane thickness < 100 nm. Preliminary measurements on membrane-based Nb-Si-Nb junctions reveal the simultaneous occurrence of tunnel behavior and Josephson coupling.

In recent years interest in semiconductor coupled weak links¹ has increased because of their potential for three-terminal superconducting devices.^{2,3} Though several of the structures developed were able to carry a large supercurrent, a detailed understanding of the mechanisms responsible for carrier transport in these structures is lacking. A device that appears to be well suited to study these mechanisms was first developed by Huang and van Duzer.⁴ It employs a thin, heavily doped silicon membrane sandwiched between superconducting electrodes. The simple geometry of this structure ensures a well-defined current path, facilitating interpretation of the measurements. In the present work we describe an improved process to fabricate large area, very thin, and flat silicon membranes and present preliminary measurements on membrane-based weak links. Advantages of the fabrication process are its relative simplicity, the well-controlled membrane thickness, and the clean, well-defined semiconductor surfaces obtained.

Thin silicon membranes can be fabricated using the etching properties of ethylenediamine-pyrocatechol-water (EPW) solutions. Anisotropic etching of (100) oriented Si wafers in EPW has been intensively investigated for a variety of purposes.⁵ The fact that the silicon etching rate in EPW is decreased by at least two orders of magnitude by the presence of a well-defined, high boron concentration allows production of membranes of nanometer thickness. Generally, a shallow boron diffusion is used to stop the EPW attack on silicon. To obtain the required doping level of about 10^{20} holes/cm³, very high dose boron diffusions into silicon are required, resulting in the presence of several unwanted surface-phase layers on the silicon.⁶ Most troublesome of these is the SiB-phase layer immediately on top of the desired heavily doped silicon surface. This layer can only be removed after having been completely oxidized. The oxidation process causes redistribution of the boron atoms, leading to an altered doping profile. As a result of this, exact control of the final thickness of the membrane in the sub-0.1 μm range is obstructed.

We show that ion implantation provides a more suitable method for doping the substrate. During the implantation process no surface-phase layers are created. Furthermore, a considerable amount of information about very shallow boron implantations has become available during the last decade,⁷ indicating the possibility of tight control

over the doping profile and consequently, over the resulting membrane thickness.

To activate implanted boron atoms and to remove implantation damage it is necessary to anneal the substrate at a minimum temperature of 900 °C. At these temperatures boron diffusion will occur and the shallow doping profile will be smeared out. BF_2^+ implantation avoids this complication as it creates an amorphous surface layer that recrystallizes at 600 °C on top of the underlying crystalline substrate. During this so-called solid phase epitaxy a large degree of activation of the dopants is achieved without diffusion, thus maintaining the as-implanted profile.

The usage of BF_2^+ offers the additional possibility of very low implantation energy. Using the lower limit of 25 keV implantation energy usually encountered in commercial implanting systems, an average implanted depth of only 20–30 nm, for B into Si, can be achieved.^{8,9}

The samples were prepared from 2 in., double side polished, 1–2.5 Ωcm *n*-type Si wafers. We report primarily on results obtained with a 65 keV BF_2^+ room-temperature implantation to a dose of 1×10^{15} ions/cm². This dose was chosen to keep the as-implanted boron concentration below the solubility limit, $2\text{--}3 \times 10^{20}$ atoms/cm³. After implantation, the samples were annealed at 800 °C for 20 min. The doping profile resulting from a SUPREM III calculation is shown in Fig. 1. As reported by Tasch *et al.*,⁹ such a calculated profile is in good agreement with secondary-ion mass spectroscopy (SIMS) data for 65 keV BF_2^+ implantations. Using the rule of thumb that EPW nearly stops etching at a boron concentration of $7\text{--}8 \times 10^{19}$ cm⁻³, we expect a membrane of about 80–90 nm to be left after EPW etching through the wafer.

Before exposing the implanted wafer to the etching solution, an EPW resistant Si_3N_4 layer is deposited on both surfaces. Square windows of $450 \times 450 \mu\text{m}^2$ are opened in the nitride layer on the undoped side of the wafer, using standard photolithography. After dipping the wafer in a 2% HF solution, the wafer is exposed to the etchant, consisting of 600 ml ethylenediamine, 96 g pyrocatechol, 160 ml water, and 3.6 g pyrazine, kept at 96–98 °C. The etch bath features a glass refluxing system to prevent composition change of EPW by loss of volatile matter, and N_2 bubbling through the solution to prevent air oxidation.

Preliminary EPW etching experiments produced membranes with a very large surface roughness that could not

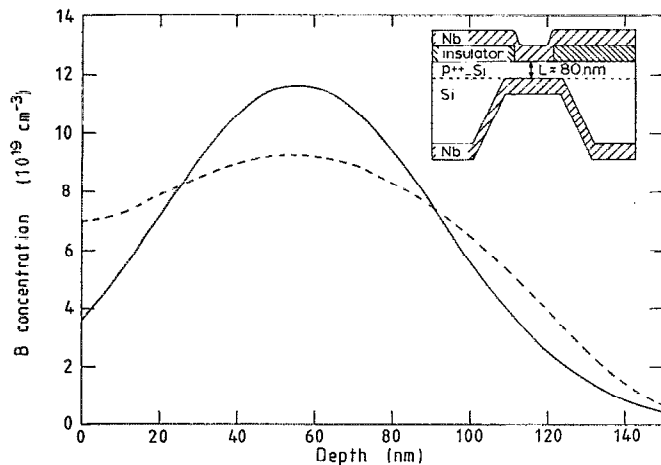


FIG. 1. Doping profiles of 65 keV BF_2^+ implantation, to a dose of $1 \times 10^{15} \text{ cm}^{-2}$, calculated by SUPREM III. Solid curve: as-implanted profile, dashed curve: doping profile after annealing at 800 °C for 20 min. The inset schematically shows the weak link structure based on the membrane obtained from this implantation plus anneal.

be eliminated by changing the EPW composition, the temperature of the solution or the N_2 flow. A two-step etching process is used to avoid this roughness problem. The first step consists of etching through most of the wafer using a 33 mass % KOH solution of 71 °C. KOH etches silicon similarly to EPW, but does not stop etching as abruptly on a high boron concentration. We find, however, that after KOH etching, the resulting membrane has a negligible surface roughness. The etching time required to produce a smooth membrane of 15 μm thick can be found from the very reproducible etch rate of 0.8 $\mu\text{m}/\text{min}$ or using optical inspection during etching. Using a 60 W lightbulb behind the wafer, the membranes become bright red when their thickness equals about 15 μm .

The second step of the etch process employs an EPW solution to etch the remaining bulk silicon and to stop at the p^{++} layer. After this shortened EPW etch, only a small surface roughness, on the order of 1 μm , occurs sometimes. This can easily be removed by overetching one or two minutes in the EPW solution. The total etching time required in EPW is best estimated by combining the etch rate of 1.0 $\mu\text{m}/\text{min}$ with optical inspection. The p^{++} layer is reached when the membranes become fully transparent.

Essential for both etching steps is the HF dip of at least 60 s just before exposing the wafer to the etchant. Omission of this dip results in irregularly shaped membranes, probably due to the presence of SiO_2 patches on the silicon surface.

Using the process outlined above, we routinely obtain $100 \times 100 \mu\text{m}^2$ silicon membranes, with a 95% yield. The thickness of these membranes was determined, by viewing a broken edge with a scanning electron microscope (SEM), to be about 80 nm. This is in good agreement with the value estimated from the doping profile shown in Fig. 1. Both high magnification optical inspection and scanning electron microscopy show the membranes to be very flat, of

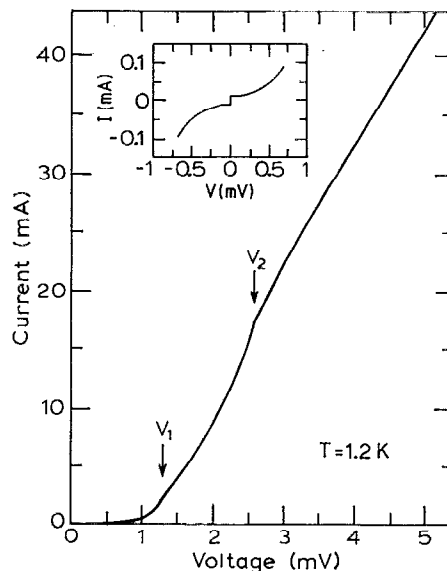


FIG. 2. IV characteristic at 1.2 K for a membrane junction. Steep rises in the current are observed at $V_1 = 1.3 \text{ mV}$ and $V_2 = 2.6 \text{ mV}$. The inset shows the presence of a small Josephson supercurrent.

uniform thickness, and pinhole free.

By using 25 keV BF_2^+ implantation we have been able to obtain membranes of an estimated thickness 30–40 nm, but no detailed information regarding their electrical properties is available yet.

A weak link structure based on an 80 nm membrane has been fabricated by electron beam evaporation of 100 nm of niobium on both sides of the membrane. The structure is shown schematically in the inset of Fig. 1. Optical inspection after niobium deposition shows the samples are still quite flat and free of pinholes.

A first measurement is shown in Fig. 2. The inset shows the presence of a small supercurrent I_c . Application of a magnetic field B results in an $I_c(B)$ characteristic resembling the familiar Fraunhofer diffraction pattern, confirming the Josephson character of the supercurrent. The larger scale IV curve displays tunneling behavior and has two prominent features at 1.3 and 2.6 meV that are possibly the first observation of multiple Andreev reflection¹⁰ in a silicon membrane. The remarkable presence of both tunneling barriers and Josephson coupling in the same sample has recently been observed in other Nb-Si-Nb structures as well.¹¹ A more detailed treatment of the phenomena observed in membrane-based weak links is in progress. Furthermore, a systematic study of supercurrent transport in silicon membranes as a function of doping concentration is now feasible. Starting with a very highly doped membrane, the required doping level can be obtained by either partial oxidation of the membrane followed by removal of the oxide, or by driving out part of the doping at high temperatures.

We thank J. J. Hangelbroek for assistance in the measurements and M. Mulder for carrying out the ion implantations. This research is supported by the Stichting voor Fundamenteel Onderzoek der Materie (FOM), which is part of the Nederlandse Organisatie voor Wetenschappelijk Onderzoek (NWO).

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